A 17 GHz Dual-Modulus Prescaler in 120 nm CMOS

Hans-Dieter Wohlmuth[1], Daniel Kehrer[1,2], Ronald Thüringer[1,2] and Werner Simbürger[1]

[1]INFINEON Technologies AG, Corporate Research, Otto-Hahn-Ring 6, D-81739 Munich, Germany,
Phone: +49 89 234-48490, Fax.: +49 89 234-47069, E-Mail: hans-dieter.wohlmuth@infineon.com

[2]Technical University Vienna, Institute of Communications and Radio-Frequency Engineering
Gusshausstrasse 25/389, A-1040 Vienna, Austria

Abstract **A completely integrated 17 GHz prescaler with programmable ratios of 4 and 5 is presented. The prescaler uses high speed differential current-mode logic and merged AND-gates. Over a band of 15 GHz the prescaler features an enhanced input sensitivity of less than 0 dBm. The circuit draws 47 mA from a single 1.5 V supply. An output buffer is also included in the circuit to drive 50 Ω loads. The circuit is manufactured in a 120 nm CMOS technology.**

I. Introduction

High speed programmable prescaler ICs are critical functional blocks in frequency synthesizers. These type of prescalers with two selectable divide ratios are used to extend the frequency range of programmable prescalers. For this application two divide ratios differing by one (P and P+1) are desirable.

To date, impressive results have been achieved with realizations in GaAs [1] and SiGe bipolar [2]. In contradiction CMOS P/P+1 prescalers have achieved operation frequencies in the range of typically 5 GHz [3]. However, the fastest of these, more than divide by two prescalers, use fixed divide ratios [4], [5] or tricky modified logic [6] (14 GHz) which requires feedback networks between the latches.

We have designed a dual-modulus divide by 4/5 prescaler, which is the core of high speed PLL systems. This circuit is optimized for high speed and high sensitivity operation. The circuit uses static CML logic for maximum bandwidth. Inputs and outputs are designed for differential operation in a 50 Ω measurement system.

II. Circuit Design

Figure 1 shows the block diagram of the prescaler. The prescaler is based on a widely-used architecture which consists of a synchronous divide-by-four/divide-by-five stage. The overall prescaler ratio is 4 or 5, depending on the level of the Modulus Control (MC) signal.

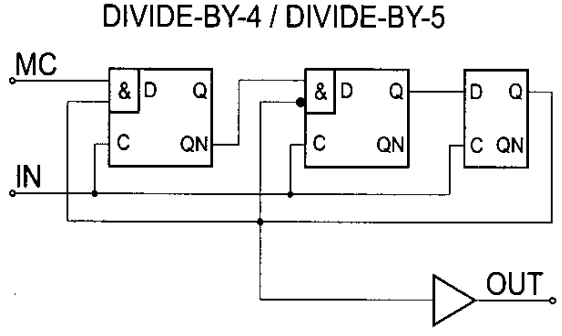

Fig. 1. Prescaler block diagram

This prescaler consists of three flip-flops and requires two additional AND gates in the signal path to allow selection of the divide ratio. These gates reduce the maximum operating frequency compared to a conventional divider circuits with fixed divide ratio. As shown in figure 1 the flip-flops and the AND gates are merged to omit additional gate delays. This leads to a higher operating speed compared to the conventional topology. A

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separate output buffer decouples the prescaler core from the 50 Ω surrounding.

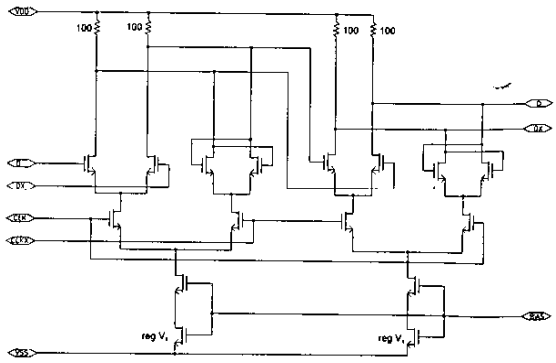

Fig. 2. Master-slave flip-flop

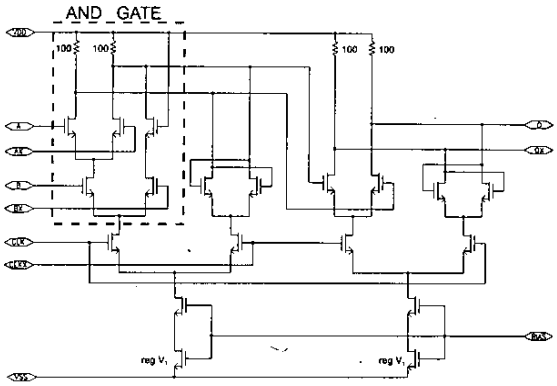

Fig. 3. Master-slave flip-flop with merged AND gate

Input stage matching is realized with 160 Ω and 240 Ω resistive on-chip divider, which also acts as a DC level shifter and ESD protection [7]. This input DC level is 0.9 V and was optimized for fast switching.

In figure 2 the master-slave flip-flop is shown. All transistors in the latches data path are of the same size and are 3/5 the width of the clock transistors. This larger clock devices increase the input sensitivity. In the high frequency part low V_T NMOS devices are used, because of their higher speed compared to PMOS transistors. 100 Ω Poly-silicon resistors are used as low capacitive loads for the latches. The simulated internal voltage swing is typical two times 600 mV_{pp}.

The current sources consist of two stacked NMOS transistors with a gate length of 180 nm. The upper transistor is a low-V_t device and the bottom is a regular-V_t device. This results in a flat current source characteristic above 0.4 V drain voltage.

The significant increase of the operating speed is achieved by using merged AND-gate flip-flops. At the same time the power consumption is reduced because the two current sources required for the separate AND gates can now be omitted. This principal is shown in figure 3. The CML AND-gate is connected in series to the clock transistor and introduces an additional logic function to the master-slave flip-flop. To ensure a symmetrical transfer function of the AND-gate a cascode transistor is used on the right data path (input BX).

The multiple stage output buffer in figure 4 is used to create sufficient output voltage swing. It consists of a pair of differential amplifier stages. In each stage the tail current is three times the current of the previous stage. The last differential amplifiers are designed to provide enough voltage swing over the 50 Ω load. The differential output stage uses internal 70 Ω resistors for DC biasing and output matching. This on-chip matching resistors reduce the output reflections and ensure sufficient bandwidth for the nearly rectangle output waveform.

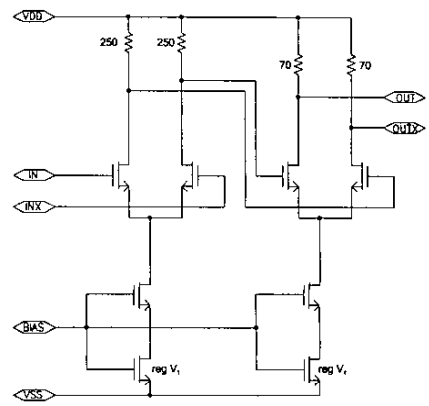

Fig. 4. Output buffer circuit diagram

Differential signals are used throughout the prescaler to achieve high noise immunity. Furthermore all interconnects are kept as short as possible. Especially the lines between slave outputs and master inputs are affecting the maximum operation frequency, due to their capacitive load. The input sensitivity of the prescaler is sufficient without an additional amplifier at the input. A simple and robust bias network generates the bias voltages for the current sources used in all flip-flops.

III. Technology

The circuit is fabricated in a 120 nm CMOS technology with six-layer copper metallization. The chip size is mainly $0.47 \times 0.49\,mm^2$. The chip size is determined by the pad frame and not by the active area, which is only a fraction of the total chip area. Figure 5 shows a micrograph of the prescaler. During fill structures in all metal layers, only diffuse outlines could be displayed. The manufactured NMOS transistors have a cut-off frequency f_T of 100 GHz and a maximum oscillation frequency f_{max} of 50 GHz, respectively [8].

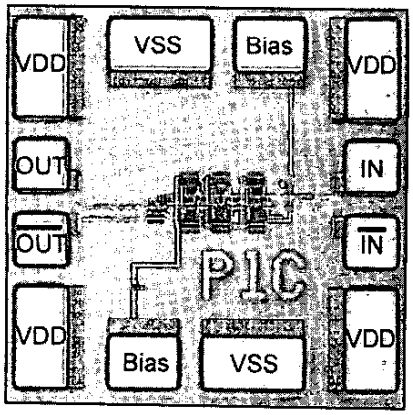

Fig. 5. Chip micrograph ($0.47 \times 0.49\,mm^2$)

IV. Experimental Results

To evaluate the circuit performance the chip was mounted on a $30 \times 30\,mm^2$ 0.51 mm RO4003 microwave substrate ($\varepsilon_r = 3.38$) with SMA connectors for input and output signals. Figure 6 shows this evaluation board mounted on a high frequency test fixture. The measured data represents the performance of the prescaler and includes the loss caused by the bond wires, microstrip lines on the test board, RF connectors and the 180° hybrid coupler. The differential input signal was generated by a 180° hybrid coupler.

Figure 7 gives the input sensitivity versus input frequency. The circuit shows broadband performance up to operation frequencies of 15 GHz with input levels less than 0 dBm. At 1.5 V power supply the maximum operation frequency of 17 GHz is achieved. This is the highest operating frequency reported so far for a dual-modulus prescaler in CMOS. The highest input sensitivity depending on the division ratio is measured at 13 GHz

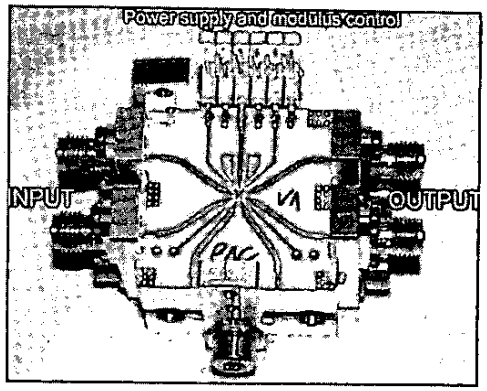

Fig. 6. High frequency test fixture $30 \times 30\,mm^2$

or 14.5 GHz respectively. The loss of sensitivity below 2 GHz is caused by the lower cut off frequency of the hybrid coupler and the limited slew rate of the sinusoidal input signal. At low frequencies a square wave signal should be applied, to reach the maximum bandwidth.

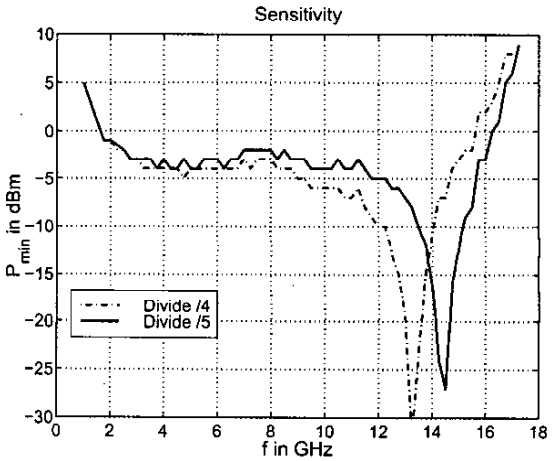

Fig. 7. Measured prescaler sensitivity versus input power

Figure 8 shows the output transient signals at 17 GHz input frequency. The measured single-ended output voltage swing on an external 50 Ω load is about $200\,mV_{pp}$.

The total supply current is 47 mA at 1.5 V. Because the flip-flop and the output buffer share the VSS and VDD pads, the individual currents could not be measured. According to simulation results, the prescaler divide by 4/5 core draws 36 mA, the output buffer 9 mA, and the bias network 2 mA from a single 1.5 V supply.

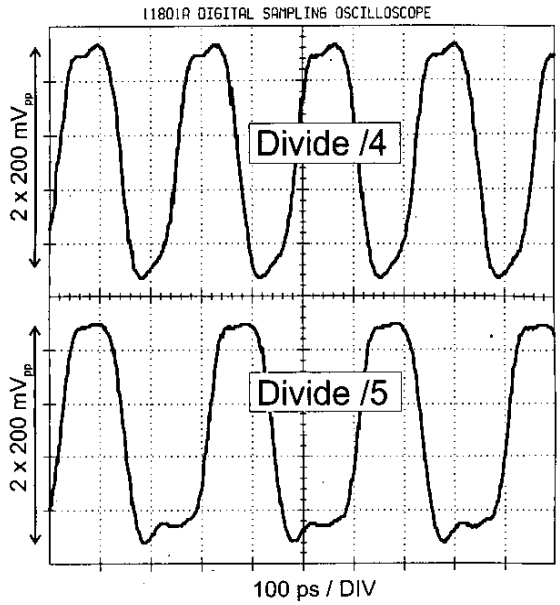

Fig. 8. Measured single ended output waveforms at 17 GHz input frequency

At this supply voltage, the prescaler consumes 70.5 mW. Table I gives a summary of the prescaler data

Maximum input frequency	17 GHz
Output voltage	2 x 200 mV_{pp}
Divide ratios	4 / 5
Supply voltage	1.5 V
Supply current	47 mA
Chip size	0.47 x 0.49 mm^2
Technology	120 nm CMOS

TABLE I. Technical data

V. Conclusions

We have presented a fully integrated high speed 4/5 prescaler in 120 nm standard CMOS, which operates up to 17 GHz. The prescaler features high input sensitivity, 50 Ω output buffer and does not require any external adjustments. To the author's knowledge, this is the highest reported value so far for a dual modulus prescaler realized in a CMOS technology.

Acknowledgments

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